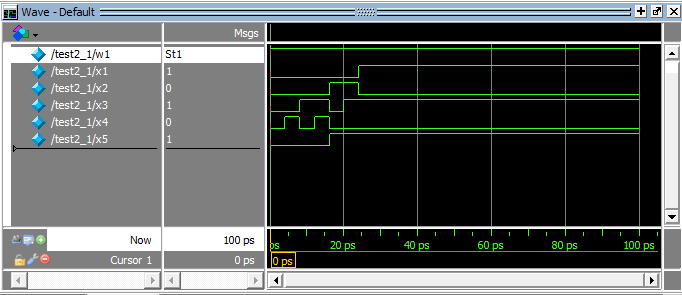
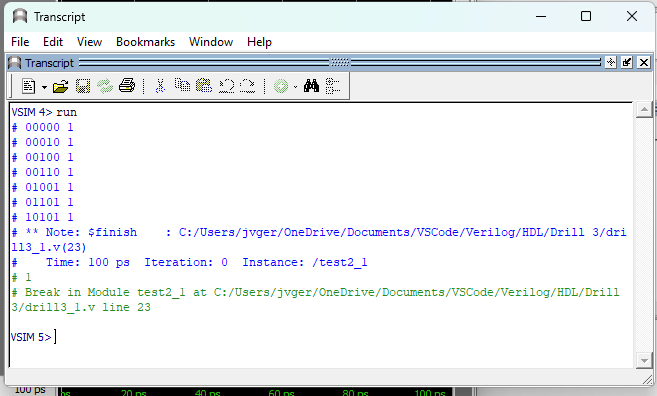
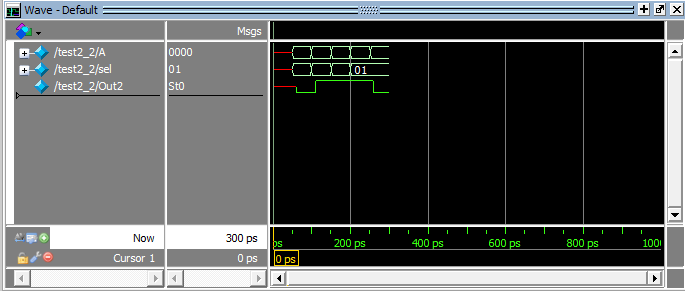
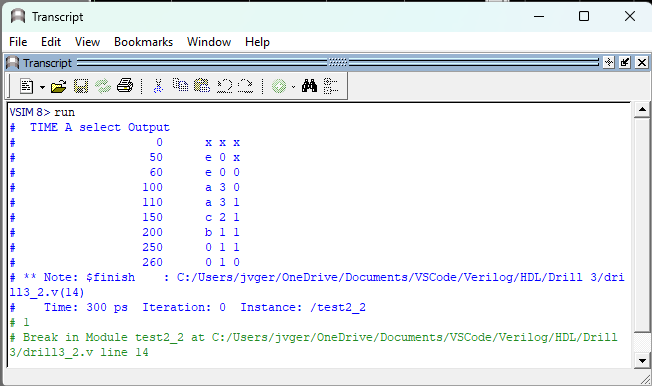
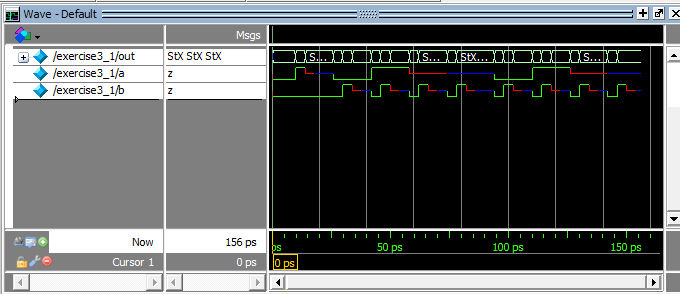
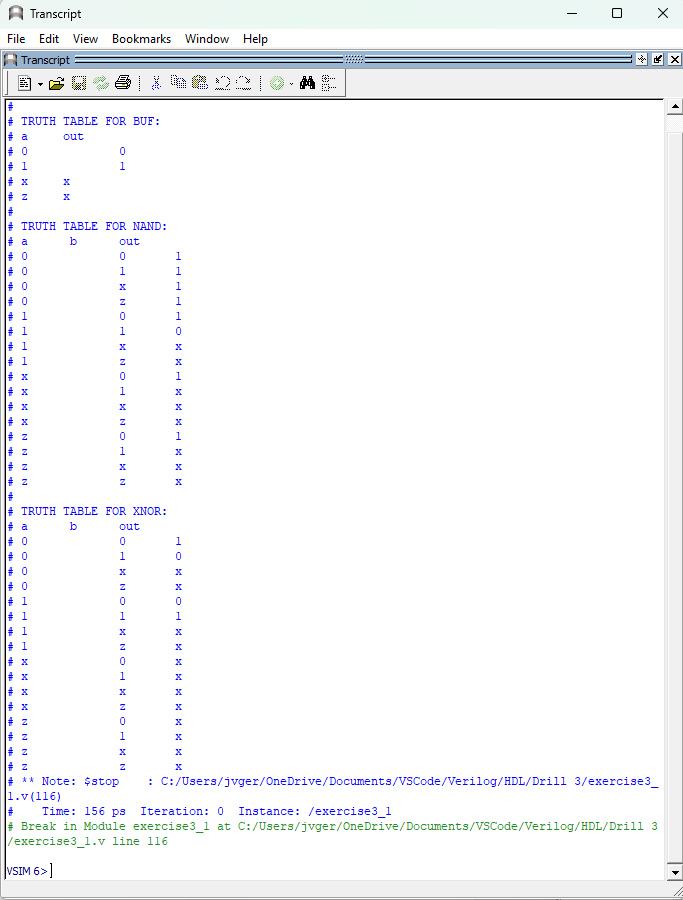
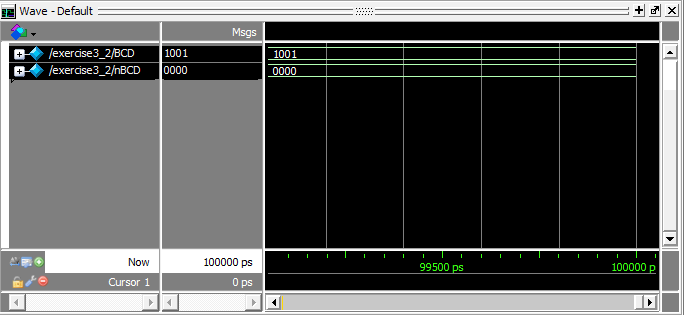
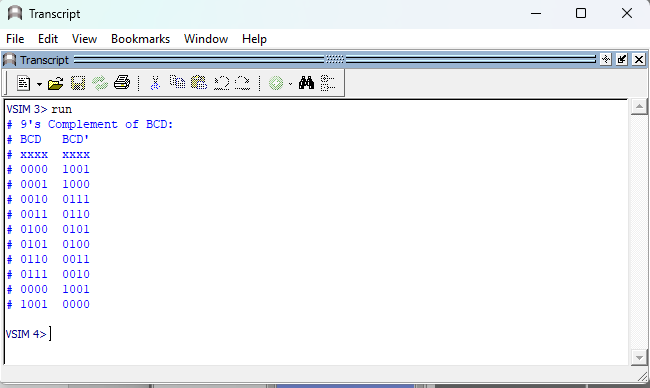
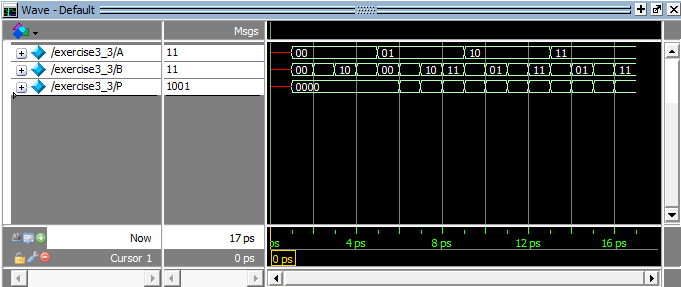
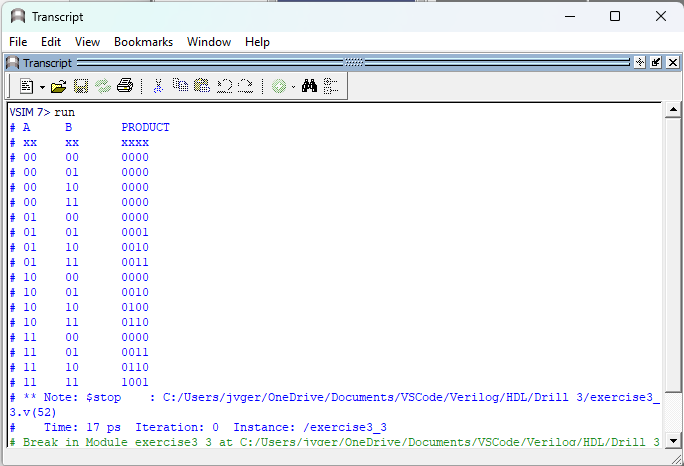
DRILL 3

* **Drill3\_1.v**
  + Testbench
  + Transcript
* **Drill3\_2.v**
  + Testbench
  + Transcript
* **Exercise3\_1.v**
  + Testbench
  + Transcript



* **Exercise3\_2.v**
  + Testbench
  + Transcript
* **Exercise3\_3.v**
  + Testbench
  + Transcript



**Review Questions**

1. **What is the difference between vectors X [5:0] and X [0:5]?**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUTS** | | | | |
|  |  | **0** | **1** | **x** | **z** |
| **XNOR** | **0** | **1** | **0** | **x** | **x** |
| **1** | **0** | **1** | **x** | **x** |
| **x** | **x** | **x** | **x** | **x** |
| **z** | **x** | **x** | **x** | **x** |
| **NAND** | **0** | **1** | **1** | **1** | **1** |
| **1** | **1** | **0** | **x** | **x** |
| **x** | **1** | **x** | **x** | **x** |
| **z** | **1** | **x** | **x** | **x** |
| **NOR** | **0** | **1** | **0** | **x** | **x** |
| **1** | **0** | **0** | **0** | **0** |
| **x** | **x** | **0** | **x** | **x** |
| **z** | **x** | **0** | **x** | **x** |
| **BUF** | **out** | **0** | **1** | **x** | **x** |

1. **How do gate delays affect the simulated output of a gate model program??**

*If there are delays in the gate, it will cause a disruption in the simulation of the gate model program because synchronization between the gates in the model is necessary.*

1. **What are the advantages and disadvantages of using gate-level models?**

*Gate-level models have the benefit of enabling the verification of timing and synthesis, but they also have a drawback in that simulating gate-level models can be slow and challenging to debug compared to non-gate level models.*